Using SystemC for high-level synthesis and integration with TLM

Presented at India SystemC User Group (ISCUG)
http://www.iscug.in

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Mike Meredith – VP Strategic Marketing
Forte Design Systems
Agenda

- **High-level synthesis**
  - A brief history of high-level synthesis
  - What is HLS?
  - HLS Basics

- **Synthesizability**
  - Introduction to the synthesizable subset standard draft
  - Recommendations and extensions

- **Keys to raising abstraction level**
  - Implicit state machine vs explicit state machine
  - Design exploration
  - HLS and Arrays
  - HLS and I/O protocols

- **Integrating synthesizable code in TLM models**

- **User Experience**
A Brief History Of High-level Synthesis
What’s In A Name?

Behavioral Synthesis

High-level Synthesis

Algorithmic Synthesis

ESL Synthesis
Synthesizing Hardware From A High-level Description -- Not a New Idea!

- **Generation 0 - Research**
  - 1970’s - 1990
  - First mention (that I can find) - 1974
    - CMU: Barbacci, Siewiorek “Some aspects of the symbolic manipulation of computer descriptions”
  - A sampling of key researchers:
    - Thomas, Paulin, Gajski, Wakabayashi, DeMann
  - Academic implementations
    - 1979 CMU - CMU-DA
    - 1988 Stanford Hercules
  - Most research focused on scheduling and allocation for datapath-dominated designs
• **First Industrial Tools**
  – NEC Cyber Workbench - 1993 (internal to NEC)
  – Synopsys Behavioral Compiler - 1994
  – Cadence Visual Architect - 1997
  – Mentor Monet - 1998

• **Challenges**
  – Synthesis direct to gates
  – HDL’s are not good behavioral algorithm languages
  – Poor quality of results
    • Area and timing closure
  – Verification difficulty
    • Interface synthesis not good
    • I/O cycle accuracy not guaranteed
• “Bloom” of industrial implementations
  – Forte Cynthesizer
  – Celoxica Agility Compiler
  – Mentor Catapult
  – Synfora Pico Express
  – Cadence C to Silicon Compiler

• Reasons for success
  – Adoption of C & C variants for input give access to algorithm code
  – Adoption of flows that include trusted logic synthesis tools
  – Quality of results caught up with hand-coded
  – Verification considered along with design
  – Designs getting too big for RTL
Why RTL Productivity Isn’t Enough (Hint: Moore’s Law)

Figure 1: Rising cost of IC design and effect of CAD tools in containing these costs. [Courtesy: Andrew Kahng, UCSD and SRC]
What Is High-level Synthesis
What Is High-level Synthesis?
It’s all about abstraction

- **Y-chart**
  - Gajski & Kuhn
  - Captures relationships between specification domains and abstraction levels

Logic Synthesis:
Register-transfer → Gates/Flipflops
Functional Block level → Logic level

High-level Synthesis:
Datapath: Algorithms → ALUs/Registers
Control: Algorithms → Register-transfer
Algorithmic level → Functional Block level
What is High-Level Synthesis?

HLS takes abstract descriptions and adds detail to produce RTL.
What is High-Level Synthesis?

• HLS creates hardware from un-timed algorithm code
  – Synthesis from a behavioral description

• Input is much more abstract than RTL code
  – No breakdown into clock cycles
  – No explicit state machine
  – No explicit memory management
  – No explicit register management
  – The high-level synthesis tool does all of the above
High-Level Synthesis is *not*...

- ... the same as writing software
  - the algorithm may be the same, but the implementation is *very* different
  - the cost/performance tradeoffs are different
  - e.g. use of large arrays
    - Software can assume essentially infinite storage with equal (quick) access time
    - Hardware implementations must tradeoff storage size vs. access time
      - these in turn affect the coding style used for synthesis

- ... the same as writing RTL
  - the input code is much more abstract
### Decisions made by designer

- **Function**
  - As implicit state machine

- **Performance**
  - Latency, throughput

- **Interfaces**

- **Storage architecture**
  - Memories, register banks etc

- **Partitioning into modules**

### Decisions made by HLS

- **State machine**
  - Structure, encoding

- **Pipelining**
  - Pipeline registers, stalling

- **Scheduling**
  - Memory I/O
  - Interface I/O
  - Functional operations
What is High-level Synthesis Used For?

- **Datapath dominated designs**
  - Most of the design is computation oriented
  - Image processing
  - Wireless signal processing

- **Control dominated designs**
  - Most of the design is making decisions and moving data
  - SSD controllers
  - Specialized processor development
  - Network switching applications

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Statistics – Real-world usage

- **Block / Module size**
  - Common = 30K → 300K gates
  - Largest we have seen = 750K gates

- **Blocks per Project**
  - Typical
    - Depends on customer stage of adoption
    - Common = 1-8
  - Largest we have seen = 200+ blocks

- **Project size**
  - (implemented with Cynthesizer)
  - Largest we have seen = 15M gates

- **QOR (Area)**
  - Typically 5-20% improvement over hand-RTL
Adopting HLS

*Productivity values and expectations*

![Diagram showing development time and area comparison between HLS and RTL design techniques.](image)

The Panic Zone

Feature Complete 2x-4x over target

Feature Complete 20% over target

Estimated Target Area

HLS Design

RTL Design

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Keys to HLS Raising Abstraction

- Implicit state machine
  - More like algorithm code
  - Leaves room for exploration

- Design exploration
  - Same source can produce designs for different purposes

- Array handling
  - Arrays can be implemented in multiple ways
  - HLS schedules memory protocol signals w/ algorithm

- Handling I/O protocols
  - HLS schedules I/O protocol signals w/ algorithm
  - Modular interfaces allow protocol encapsulation & reuse
High-level Synthesis Basics
High-level Synthesis Basics

• High-level synthesis begins with an algorithmic description of the desired behavior
• Behavior is expressed in a high level language
• SystemC is the input language for Cynthesizer
• The second input is the ASIC or FPGA technology library
  – Cell functions, area and timing
• The third input is directives for synthesis
  – Target clock period (required)
  – Other directives: pipelining, latency constraints, memory architecture
Consider the following behavioral description to be synthesized for a 100MHz clock period:

```c
typedef unsigned char bit8;
unsigned long example_func( bit8 a, bit8 b, bit8 c,
                           bit8 d, bit8 e )
{
    unsigned long y;
    y = ( ( a * b ) + c ) * ( d * e );
    return y;
}
```

- This description is *un-timed*: The user does not specify the clock boundaries
  - Does not specify the latency
  - Does not specify which values are registered or when to compute each value
- Cynthesizer will map the SystemC/C++ operations (‘*’, ‘+’) to datapath components, and add clock boundaries
  - Driven by target clock period and other directives
  - Results in known latency and registers
  - Depends on technology library
High-level Synthesis Example: Control & Data Flow Graph

- **Cynthesizer analyzes the source and determines:**
  - Inputs & Outputs
  - Operations
  - Data dependencies

- **A control/dataflow graph (CDFG) is constructed:**
  - With no timing information
  - Represents the data flow for the functionality of the design

- **The graph shows data dependencies:**
  - Operations that must complete before others can begin
    - e.g. \((a*b)\) must complete before we can calculate \((a*b)+c\)

- **The graph shows control dependencies:**
  - if/else constructs will turn into select operations

```plaintext
if (x == 0)
    q = d1;
else
    q = d2;
```
High-level Synthesis Example: Control & Data Flow Graph

The control/dataflow graph (CDFG) analysis would construct the following structure from `example_func()`:

![Diagram of CDFG analysis](image)

- `a` connected to `16` and `16` connected to `x^1`
- `b` connected to `8`
- `c` connected to `8`
- `d` connected to `x^2`
- `e` connected to `8`
- `x^1` connected to `+1` and `+1` connected to `t1`
- `t1` connected to `17`
- `t2` connected to `16`
- `x^2` connected to `x^3`
- `x^3` connected to `33` and `33` connected to `y`

The diagram shows the flow of data and operations, with nodes representing operations and edges representing data flow. The CDFG analysis results in a structured representation of the control and data flow for the function `example_func()`. The diagram includes nodes labeled with variables and operations, along with the flow of data indicated by the edges.

The process involves several stages:
- **Lexical Processing**
- **Algorithm Optimization**
- **Control/Dataflow Analysis**
- **Library Processing**
- **Scheduling & Binding**
- **Design Evaluation**
- **Output Generation**
High-level Synthesis Example: Library Processing

Assume the characterized library has the following functional units available

<table>
<thead>
<tr>
<th>Functional Unit</th>
<th>Delay</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8=16</td>
<td>2.78 ns</td>
<td>4896.5</td>
</tr>
<tr>
<td>16+16=17</td>
<td>1.99 ns</td>
<td>1440.3</td>
</tr>
<tr>
<td>20x20=40</td>
<td>5.88 ns</td>
<td>27692.6</td>
</tr>
</tbody>
</table>

An initial allocation might be:
- Two “8x8=16” multipliers
- One “16+16=17” adder
- One “20x20=40” multiplier
High-level Synthesis Example: Scheduling

- Using the initial allocation the initial schedule would be:

<table>
<thead>
<tr>
<th>Operator</th>
<th># Needed</th>
<th>Cycle1</th>
<th>Cycle2</th>
<th>Cycle3</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8=16</td>
<td>2</td>
<td>( t_1 = a \times b )</td>
<td>( t_2 = d \times e )</td>
<td></td>
</tr>
<tr>
<td>16+16=17</td>
<td>1</td>
<td>( t_3 = t_1 + c )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20x20=40</td>
<td>1</td>
<td></td>
<td></td>
<td>( y = t_2 \times t_3 )</td>
</tr>
</tbody>
</table>

- Total functional unit area =
  \[ (2 \times 4896.5) + 1440.3 + 27692.6 = 38925.9 \]

- Delays fit within 100 MHz clock
High-level Synthesis Example: Scheduling (cont.)

Scheduling notes that the $d*e$ operation can be moved to cycle 2 to eliminate one 8x8 multiply operator

<table>
<thead>
<tr>
<th>Operator</th>
<th># Needed</th>
<th>Cycle1</th>
<th>Cycle2</th>
<th>Cycle3</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8=16</td>
<td>1</td>
<td>t1=a*b</td>
<td>t2=d*e</td>
<td></td>
</tr>
<tr>
<td>16+16=17</td>
<td>1</td>
<td></td>
<td>t3=t1+c</td>
<td></td>
</tr>
<tr>
<td>20x20=40</td>
<td>1</td>
<td></td>
<td></td>
<td>y=t2*t3</td>
</tr>
</tbody>
</table>

- **Total functional unit area** = 
  4896.5 + 1440.3 + 27692.6 = 34029.4

- **Delays fit within 100 MHz clock**
High-level Synthesis Example: Binding

- Binding assigns specific instances of functional units to the required operators
- Further optimization binds the 8x8 multiply operations to the 20x20 multiplier instance

```
Operator  # Needed  Cycle1  Cycle2  Cycle3
16+16=17  1         t3=t1+c
20x20=40  1         t1=a*b  t2=d*e  y=t2*t3
```

- Total functional unit area = 1440.3 + 27692.6 = 29132.9
- Delays fit within 100 MHz clock
High-level Synthesis Example: Output Hardware Structure

Note: Implicit state machine input produces explicit state machine output

Lexical Processing
Algorithm Optimization
Control/Dataflow Analysis
Library Processing
Scheduling & Binding
Design Evaluation
Output Generation

Mux selects come from the FSM

Multiplier 20x20=40
Adder 16+16=17

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Introduction To The SystemC Synthesizable Subset Draft Under Development

March 2013
SystemC Synthesizable Subset Work

- Development of a description of a synthesizable subset of SystemC
- Started in the OSCI Synthesis Working Group
- Current work is in Accellera Systems Initiative Synthesis Working Group

- Many contributors over a number of years
- Broadcom, Cadence, Calypto, Forte, Fujitsu, Global Unichip, Intel, ITRI, Mentor, NEC, NXP, Offis, Sanyo, Synopsys
General Principles

- Define a meaningful minimum subset
  - Establish a baseline for transportability of code between HSL tools
  - Leave open the option for vendors to implement larger subsets and still be compliant

- Include useful C++ semantics if they can be known statically – eg templates
Scope of The Planned Standard

- Synthesizable SystemC
- Defined within IEEE 1666-2011
- Covers behavioral model in SystemC for synthesis
  - SC_MODULE, SC_CTHREAD, SC_THREAD
- Covers RTL model in SystemC for synthesis
  - SC_MODULE, SC_METHOD
- Main emphasis of the document is on behavioral model synthesizable subset for high-level synthesis
Scope Of The Planned Standard

**SystemC Elements**
- Modules
- Processes
  - SC_CTHREAD
  - SC_THREAD
  - SC_METHOD
- Reset
- Signals, ports, exports
- SystemC datatypes

**C++ Elements**
- C++ datatypes
- Expressions
- Functions
- Statements
- Namespaces
- Classes
- Overloading
- Templates
High-level Synthesis With SystemC In The Design Flow

- Design and testbench converted to SystemC modules or threads
- Design
  - Insertion of signal-level interfaces
  - Insertion of reset behavior
  - Conversion to SC_CTHREADs
- Testbench
  - Insertion of signal-level interfaces
  - Reused at each abstraction level
    - Behavioral
    - RTL
    - Gate

Diagram:
- SystemC Module
- Behavioral Simulation
- SystemC Testbench
- Software “Model”
- High-level Synthesis
- Optimize
- Functional Simulation
- Logic Synthesis
- RTL

Synthesis

Software “Model”

SystemC Module

Behavioral Simulation

SystemC Testbench

High-level Synthesis

Optimize

Functional Simulation

Logic Synthesis

RTL

Behavioral

RTL

Gate
Module Structure for Synthesis

- **Ports required for SC_CTHREAD, SC_THREAD**
  - clock
  - reset

- **Signal-level ports for reading data**

- **Signal-level ports for writing data**

**SC_MODULE**

- **SC_CTHREAD**
- **SC_THREAD**
- **SC_METHOD**

**Submodule**

**Signals**

**Member functions**

**Data members (Storage)**
Module Declaration

- **Module definition**
  - SC_MODULE macro
    - or
  - Derived from sc_module
    - class or struct
  - SCCTOR
    - or
  - SC_HAS_PROCESS

// A module declaration
SC_MODULE( my_module1 ) {
    sc_in< bool> X, Y, Cin;
    sc_out< bool > Cout, Sum;
    SCCTOR( my_module1 ) {...}
};

// A module declaration
SC_MODULE( my_module1 ) {
    sc_in< bool> X, Y, Cin;
    sc_out< bool > Cout, Sum;
    SC_HAS_PROCESS( my_module1 );
    my_module1(const sc_module_name name ) :
    sc_module(name)
    {...}
};
SC_THREAD & SC_CTHREAD

Reset Semantics

- At start_of_simulation each SC_THREAD and SC_CTHREAD function is called
  - It runs until it hits a wait()

- When an SC_THREAD or SC_CTHREAD is restarted after any wait()
  - If reset condition is false
    - execution continues
  - If reset condition is true
    - stack is torn down and function is called again from the beginning

- This means
  - Everything before the first wait will be executed while reset is asserted

Note that every path through main loop must contain a wait() or simulation hangs with an infinite loop
void process() {

    // reset behavior must be executable in a single cycle
    reset_behavior();

    wait();

    // initialization may contain any number of wait()s.
    // This part is only executed once after a reset.
    initialization();

    // infinite loop
    while (true) {
        rest_of_behavior();
    }
}
Process Structure Options

- **SC_THREAD** and **SC_CTHREAD** processes must follow one of the forms shown:
  
  ```
  while( 1 )
  { }
  
  while( true )
  { }
  
  do { } while ( 1 );
  
  do { } while ( true );
  
  for ( ; ; )
  { }
  ```

- Note that there must be a `wait()` in every path of the infinite loops to avoid simulator hangup.
Specifying Clock and Reset

- Simple signal/port and level

```cpp
SC_CTHREAD(func, clock.pos());
reset_signal_is(reset, true);
areset_signal_is(areset, true);

SC_THREAD(func);
sensitive << clk.pos();
reset_signal_is(reset, true);
areset_signal_is(areset, true);

inline void reset_signal_is(const sc_in<bool>& port, bool level);
inline void reset_signal_is(const sc_signal<bool>& signal, bool level);
inline void areset_signal_is(const sc_in<bool>& port, bool level);
inline void areset_signal_is(const sc_signal<bool>& signal, bool level);

For synthesis, SC_THREAD can only have a single sensitivity to a clock edge.
Use Of wait()

- For synthesis, `wait(...)` can only reference the clock edge to which the process is sensitive

- For `SC_CTHREADs`
  - `wait()`
  - `wait(int)`

- For `SC_THREADs`
  - `wait()`
  - `wait(int)`
  - `wait(clk.posedge_event())`
  - `wait(clk.negedge_event())`

For synthesis of `SC_THREADs`, `wait(event)` must match the sensitivity of the clock edge.
## Types and Operators

- **C++ types**
  - `sc_int`, `sc_uint`
  - `sc_bv`, `sc_lv`
  - `sc_bignum`, `sc_biguint`
  - `sc_logic`
  - `sc_fixed`, `sc_ufixed`

- All SystemC arithmetic, bitwise, and comparison operators supported
- Note that shift operand should be unsigned to allow minimization of hardware

### Supported SystemC integer functions

<table>
<thead>
<tr>
<th>bit select</th>
<th>part select (i,j)</th>
<th>concatenate (,)</th>
<th>to_int()</th>
<th>to_long()</th>
<th>to_int64()</th>
<th>to_uint()</th>
<th>to_uint64()</th>
<th>to_ulong()</th>
</tr>
</thead>
<tbody>
<tr>
<td>iszero()</td>
<td>sign()</td>
<td>bit()</td>
<td>range()</td>
<td>length()</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>reverse()</td>
<td>test()</td>
<td>set()</td>
<td>clear()</td>
<td>invert()</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Data Types

- **C++ integral types**
  - All C++ integral types except `wchar_t`
  - `char` is signed (undefined in C++)

- **C++ operators**
  - `a>>b`
    - Sign bit shifted in if `a` is signed
  - `++` and `--` not supported for `bool`

- “X” has limited support for synthesis
  - A tool MAY use “X” to specify an explicit don't-care condition for logic synthesis

- "Z" has limited support for synthesis
  - Supported only if it appears in an expression assigned directly to a port variable
Pointers

- **Supported for synthesis**
  - “this” pointer
  - “Pointers that are statically resolvable are supported for synthesis. Otherwise, they are not supported.”
  - If a pointer points to an array, the size of the array must also be statically determinable.

- **Not Supported**
  - Pointer arithmetic
  - Testing that a pointer is zero
  - The use of the pointer value as data
    - eg hashing on a pointer is not supported for synthesis
Other C++ Constructs

- **Supported**
  - const
  - volatile
  - namespace
  - enum
  - class and struct
    - private, protected, public
  - Arrays
  - Overloaded operators

- **Not supported**
  - sizeof()
  - new()
    - Except for instantiating modules
  - delete()
  - typeid()
  - extern
  - asm
  - Non-const global variables
  - Non-const static data members
Join A Working Group And Contribute!

SystemC Synthesis Working Group (SWG)

Charter

This group is responsible for the definition of a synthesizable subset of SystemC.

Chair: Andres Takach, Mentor Graphics
Vice-Chair: Michael Meredith, Forte Design Systems

Background

In August 2009, this group released the Synthesis Subset Draft 1.3 standard synthesis subset draft for public review. The draft features several technical updates. Supported language constructs are now established, and a chapter on processes, clocks, and resets has been added. The draft also includes a discussion on abstraction levels that puts the concepts of the synthesizable subset in the context of the abstraction levels defined for TLM.

Public review of the draft is now closed. The draft is available for download here.

Join this Working Group

If you are an employee of a member company and would like to join this working group, click here (requires login) and click Join Group. WG participation requires right of entry by the group chair.
Synthesizability
Recommendations & Extensions
• HLS tools can handle pointers in the C++ code

```cpp
// Passing a pointer to array
void func1(int *a) {
    for (i = 0; i < N; i++)
        sum += a[i];
}
```

• But a pointer needs to be resolved to a specific array (or variable) in the design at compile time

```cpp
// OK to call with a determinate //pointer
ptr = arr1;
func1(ptr);
ptr = arr2;
func1(ptr);

// Not OK to call with an //indeterminate pointer
if (external_input.read() == 1)
    ptr = arr1;
else
    ptr = arr2;
// array used depends on //external input
func1(ptr); // ERROR
```
Reset Logic Recommendations

• The reset logic code block *should*:  
  – Write the reset value to all output ports  
    • e.g. my_port.write(0) for a standard SystemC sc_out port  
  – Call the `reset()` function of all modular interface ports that have one  
    • cynw_p2p ports (din.reset(), dout.reset())  
    • Memory ports for explicit memories  
  – Write the reset value to all variables  
    • An array cannot be initialized in one cycle unless it is flattened

• The reset logic code block *should not*:  
  – Access a memory (e.g. an un-flattened array)  
  – Call a function that calls `wait()`  
    (e.g. cannot call the `get()` function of a cynw_p2p input port)  
  – Such multi-cycle code should be executed after the reset protocol block
Data Type Recommendations

- Correct sizing of variables will have a big impact on area
  - Particularly on ports!
  - Affects not just the variable but all operations on it

- Cynthesizer can often *automatically* determine the optimum bit width for a variable
  - *Only if* it can determine the maximum value

- Replacing C++ built-in types with `sc_int` or `sc_uint` types enforces desired sizing of hardware
  - It helps when Cynthesizer cannot determine maximum values
  - Allows selection and testing of individual bits and ranges
    ```cpp
    sc_uint<32> status; // 32-bit register
    if (status[7] == 1) // test individual bits
        count = status.range(3,0); // get a range of bits
    ```

- C++ semantics sometimes force data values to 64 bits
  - Casting to a narrower type can avoid this
Cynthesizer Fixed Point Support

- Cynthesizer supports synthesis of fixed point arithmetic

```cpp
sc_fixed<wl, iwl, q_mode, o_mode, n_bits> Object_Name;
sc_ufixed<wl, iwl, q_mode, o_mode, n_bits> Object_Name;
```
- *wl*: “word length” Total number of bits used
- *iwI*: “integer word length.” Number of bits to left of the decimal point
- *q_mode*: “quantization mode” Represents the process to be done when the value can not be represented precisely.
- *o_mode*: “overflow mode” (SC_WRAP、SC_SAT、)
- *n_bits*: is used in overflow processing

- Forte provides an sc_fixed compatible class for improved simulation speed
Cynthesizer Floating Point Support

- Cynthesizer supports floating point types
  - Use cynw_cm_float<> an optional library if it is necessary to synthesize float/double.

```
cynw_cm_float<E,M,D,N,EX,R> object_name, ...;
E : The number of bits for exponent (For single precision:8)
M : The number of bits for Mantissa (For single precision:23)
D : 1 use denormal numbers for gradual underflow (default 1)
N : When set to 1, interpret NaN, Inf according to IEEE 754 (default 1)
EX : When set to 1, generate IEEE 754 exceptions (default 0)
R : Rounding (Default : CYNW_NEAREST)
```

Example:
```
#include "cynw_cm_float.h"

cynw_cm_float<8,23> a, b, c;  // IEEE Single Precision Format
...
  a = b + c;
  a = b * c;
```
Cynthesizer Complex Class Support

- **Cynthesizer includes a synthesizable complex datatype**
  - API compatible with std::complex
  - Just use std::complex in your code, the synthesizable implementation will be used

```cpp
#include <complex>

typedef cynw_fixed< W, L, SC_RND > my_fp;

typedef std::complex< my_fp > my_cplx;

my_cplx out, a, b, c, d;
out = (a * b) + (c * d);
```

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Keys To Raising Abstraction Level
Keys to Raising Abstraction

• **Implicit state machine**
  – More like algorithm code
  – Leaves room for exploration

• **Design exploration**
  – Same source can produce designs for different purposes

• **Array handling**
  – Arrays can be implemented in multiple ways
  – HLS schedules memory protocol signals w/ algorithm

• **Handling I/O protocols**
  – HLS schedules I/O protocol signals w/ algorithm
  – Modular interfaces allow protocol encapsulation & reuse
Implicit State Machine vs Explicit State Machine

- **Implicit state machine form**
  - Has a higher level of abstraction
  - Matches common algorithm description
  - Can be mapped to multiple implementations with different performance characteristics

```c
typedef unsigned char bit8;
unsigned long example_func( bit8 a, bit8 b, bit8 c, bit8 d, bit8 e )
{
    unsigned long y;
    y = ( ( a * b ) + c ) * ( d * e );
    return y;
}
```
Keys to Raising Abstraction

- **Implicit state machine**
  - More like algorithm code
  - Leaves room for exploration

- **Design exploration**
  - *Same source can produce designs for different purposes*

- **Array handling**
  - Arrays can be implemented in multiple ways
  - HLS schedules memory protocol signals w/ algorithm

- **Handling I/O protocols**
  - HLS schedules I/O protocol signals w/ algorithm
  - Modular interfaces allow protocol encapsulation & reuse
Exploration

*One source can be targeted to multiple uses*

High Level Synthesis Methodology

Directives

Cell Phone

Tablet

Theater

Courtesy Michael Bohm, Intel
Exploration Example

- Non-pipelined implementation
  vs
- Pipelined implementation (1 calculation / 2 cycles)
  vs
- Pipelined implementation (1 calculation / cycle)
// Read an input, do some calculations, write output
for (i = 0; i < N; i++)
{
    X = inp.get(); // Read input
    // Assume the arrays are flattened, so accesses take
    // zero time
    Y = (A[i] + B[i] + C[i]) * (D[i] + E[i] + F[i]) * X;
    outp.put(Y); // Write output
}

• An un-pipelined schedule:
  – Each iteration takes six cycles

--- cycle 1 ---
X = inp.get();
--- cycle 2 ---
R1 = A[i] + B[i]
R2 = D[i] + E[i]
--- cycle 3 ---
R3 = R1 + C[i]
R4 = R2 + F[i]
--- cycle 4 ---
R5 = R3 * R4
--- cycle 5 ---
Y = R5 * X
--- cycle 6 ---
outp.put(Y);

<table>
<thead>
<tr>
<th>I</th>
<th>++</th>
<th>++</th>
<th>*</th>
<th>*</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>12</td>
</tr>
</tbody>
</table>

Iteration 1  Iteration 2

<table>
<thead>
<tr>
<th>Resources</th>
<th>2 Adders, 1 Multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency</td>
<td>6 clock cycles</td>
</tr>
<tr>
<td>Throughput</td>
<td>1 I/O per 6 clock cycles</td>
</tr>
</tbody>
</table>
Types of Pipelining

- **Pipelined datapath components**
  - A multicycle computation implemented in a datapath component
  - E.g. a wide multiplier that takes 3 cycles to complete and can start a new computation every cycle
  - If a datapath component is pipelined, Cynthesizer will potentially create a schedule that starts a new computation every cycle

- **Pipelined loops**
  - A multicycle computation implemented in the FSM
  - E.g. a fir filter that takes 5 cycles to complete a computation, but can start a new computation every cycle
  - Very useful technique to improve throughput
  - When pipelined, a new loop iteration can start before the previous one ends
  - Multiple iterations of the loop are active at the same time
Pipelining Example

- Pipeline the example with an initiation interval of “2”

```
CYN_INITIATE( CONSERVATIVE, 2, "my_pipe" );
```

<table>
<thead>
<tr>
<th>Cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iteration 1</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iteration 2</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iteration 3</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iteration 4</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Resources: 2 Adders, 1 Multiplier

Latency: 6 clock cycles

Throughput: 1 I/O per 2 clock cycles

Throughput tripled with no increase in resources!
### Pipelining Example

- **Pipeline the example with an initiation interval of “1”**

  ```cyn
  CYN_INITIATE( CONSERVATIVE, 1, "my_pipe" );
  ```

<table>
<thead>
<tr>
<th>Iteration 1</th>
<th>I</th>
<th>++</th>
<th>++</th>
<th>*</th>
<th>*</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iteration 2</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
<tr>
<td>Iteration 3</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
<tr>
<td>Iteration 4</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
<tr>
<td>Iteration 5</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
<tr>
<td>Iteration 6</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
<tr>
<td>Iteration 7</td>
<td>I</td>
<td>++</td>
<td>++</td>
<td>*</td>
<td>*</td>
<td>O</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cycle</th>
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<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
</table>

**Resources** | 4 Adders, 2 Multiplier
**Latency** | 6 clock cycles
**Throughput** | 1 I/O per 1 clock cycles

*Fully pipelined for a 6x improvement in throughput for only a 2x increase in resources.*
HLS and Arrays
Keys to Raising Abstraction

- Implicit state machine
  - More like algorithm code
  - Leaves room for exploration

- Design exploration
  - Same source can produce designs for different purposes

- Array handling
  - Arrays can be implemented in multiple ways
  - HLS schedules memory protocol signals w/ algorithm

- Handling I/O protocols
  - HLS schedules I/O protocol signals w/ algorithm
  - Modular interfaces allow protocol encapsulation & reuse
Array Handling

- Array handling is a key contributor to HLS abstraction
- Arrays are accessed using normal C++ syntax
  
  ```c++
  sc_uint<8> array[6][8];
  x = (array[5][0] + array[5][1]) * array[5][3];
  ```
- Directives control how array is implemented
- If array is implemented as memory, HLS determines when to drive each protocol signal
Implementing Arrays

- **Multiple ways to implement arrays**
  - Memory
    - Storage is RAM or ROM
    - Access through port/protocol
  - Register bank
    - Storage is registers
    - Access through port/protocol
  - Flattened
    - Each array element is treated as an individual variable
    - Permits unlimited accesses per cycle
HLS and I/O Protocol
Keys to Raising Abstraction

- Implicit state machine
  - More like algorithm code
  - Leaves room for exploration

- Design exploration
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- Array handling
  - Arrays can be implemented in multiple ways
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- Handling I/O protocols
  - HLS schedules I/O protocol signals w/ algorithm
  - Modular interfaces allow protocol encapsulation & reuse
Protocol Scheduling

- Scheduling determines what operations happen in each clock cycle
- Protocol scheduling refers to the way scheduling takes I/O operations and wait()s into account
- In order to produce a good result, scheduling must satisfy these conditions
  1. Operations must be kept in order according to the dataflow graph 
     e.g. in “A = B + ( C * D )” the multiplication must be done before the addition
  2. Key relationships between I/O operations and clock edges must be maintained to preserve protocol integrity 
     e.g. address, data, and write-enable must be asserted in the same cycle for an SRAM write
Cynthesizer uses a “transaction accurate” protocol scheduling policy

- Directives are used to define groups of I/O operations and wait()s as transactions
- Within each transaction I/O operations and waits are kept in order as written
- Rules determine how transactions can move with respect to each other
- Computation operations are allowed to move wherever the dataflow graph will allow
In these protocol blocks, the RTL generated by Cynthesizer maintains the order of I/O operations (fixed I/O).

The protocol accuracy is maintained by the wait() statements embedded into the protocol blocks.
Protocol Results

For all the architectures
- Input: 8 cycles
- Output: 8 cycles
- These are un-pipelined architecture
- The cycles for processing code between I/O protocol blocks depend on the constraints

The operations involving the MEM variable gets scheduled (free scheduling) depending on the latency constraints, Library and clock frequency.

Architecture 1
- Input: 8 cycles
- Output: 8 cycles

Architecture 2
- Input: 8 cycles
- Output: 8 cycles

Architecture 3
- Input: 8 cycles
- Output: 8 cycles
Protocol + Algorithm Enables HLS Verification Flow

**HLS Flow**

- **Manual**
  - High-Level Model
  - Algorithm Verification & Primary Functional Verification
  - RTL Model
  - Check Implementation
  - Logic Synthesis
  - Netlist
  - Check Implementation

**RTL Flow**

- **Manual**
  - High-Level Model
  - Algorithm Verification
  - RTL Model
  - Primary Functional Verification
  - Logic Synthesis
  - Netlist
  - Check Implementation
Modular Interfaces

- Separate protocol behavior from functional behavior
- Improves reuse of protocol
- Improves reuse of function

Structure
- Ports
- Signals
- Connections

Function
- Protocol
- Cycle-accurate I/O behavior

Modular Interface Classes
- Socket Classes
  - Protocol APIs
- Channels
- Binding functions
Cynthesizer Interface Generator

- **The Interface Generator is a specialized tool**
  - For creating modular interfaces between modules or threads

- **The user specifies the characteristics of the interface**
  - By filling in forms in the Cynthesizer Workbench

- **The interface generator produces SystemC source code**
  - Synthesizable PIN-level versions
  - High-speed TLM versions
Cynthesizer Interface Classes

*Streaming Interfaces*

- **The p2p stream class**
  - 2-wire ready/busy handshake
  - 1 transfer per clock
  - Synchronous stalling due to starvation
  - Synchronous or asynchronous stalling due to back pressure
  - Supports fifo of memory or registers
  - Supports clock domain crossing

- **The stream class**
  - Similar to p2p stream
  - Supports writer and reader with different I/O granularities
Cynthesizer Interface Classes

Buffer Interfaces

- **Buffer class**
  - Supports single buffer, double buffer etc
  - Memory based storage

- **Circular buffer class**
  - Writer & reader share a memory
  - Manages indices for wrap around accesses
  - Stalls writer if needed to prevent overrun
  - Stalls reader if needed for starvation
Cynthesizer Interface Classes

Windowing Interfaces

- **Line buffer class**
  - For image processing applications
  - Implements moving window within a frame
  - Contains line memories
  - Implements memory index generation
  - Handles boundary conditions
Integrating Synthesizable Code In TLM Models
TLM Methodology Goals

• **Modularity**
  – Allow reuse of bus interface with multiple designs without modification
  – Allow reuse of design with multiple bus interfaces without modification
  – Maximize shared code between TLM and implementation model

• **TLM priorities**
  – Interoperability with other TLM-2 models
  – Maximum simulation speed

• **Implementation priorities**
  – All the detail needed for implementation
  – Good QoR
Forte TLM Approach

- Transform synthesis input using substitution of TLM sockets and synthesizable sockets
- Transformation using conventional C++ techniques
  - Macros, class substitution, template specialization, etc
- These techniques have been in use since 2006
  - Point-to-point, TLM-1, TLM-2
Building Modular Bus Interfaces

- **Main elements of TLM slave**
  - TLM socket
  - Address decode
    - Convenience functions `read()` and `write()`
  - Registers / Memories
  - Computation function

- **Main elements of synthesizable slave**
  - Bus ports
  - Bus protocol thread
  - Address decode
  - Registers / Memories
  - Computation function
  - Computation thread
Master/Slave with TLM Sockets

**Master**
- **Initiator socket**
  - `write()`
  - `b_transport()`

**Slave**
- **Target socket**
  - `b_transport()`
  - `compute()`
- **Decode & storage**
  - `write()`
  - `read()`

*Thread*
Master/Slave with Pin-level Sockets

PIN Level

**Master**

- **Initiator socket**
  - `write()`
- **THREAD**

**Slave**

- **Target socket**
  - **CTHREAD**
  - `compute()`
- **Decode & storage**
  - `write()`
  - `read()`
Speed Issues
To Deal With By Methodology

- Waiting for clock edges in protocols
  - Use of modular interfaces with PIN and TLM versions

- SC_CTHREAD vs SC_THREAD
  - Macro or equivalent

- wait() in reset code
  - #ifdef or equivalent

- Leaving clocks wired up without transitions
  - David Black’s noclock class

- sc_uint vs int
  - Macros/typedefs or equivalent
Forte Features Supporting TLM

• Modular interface features
  – Synthesizability of encapsulated socket classes
    • sc_in, sc_out ports
    • Binding functions
    • SC_CTHREADs and SC_METHODs in synthesizable sockets

• Automated simulation configuration
  – With automated switching between TLM and PIN-level

• IP
  – TLM support in all point-to-point and generated interface IP
  – Methodology examples
    • TLM-1, TLM-2
    • APB, AHB, AXI
User Experience
Synthesizing SystemC to Layout

High Level Synthesis Methodology

Directives

Michael A. Bohm
Intel
6/3/2012
Why are companies moving to High Level Synthesis with SystemC?

<table>
<thead>
<tr>
<th>Aspect</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Faster time to RTL</td>
<td>64%</td>
</tr>
<tr>
<td>Faster verification time</td>
<td>49%</td>
</tr>
<tr>
<td>Fewer engineering resources</td>
<td>31%</td>
</tr>
<tr>
<td>Fewer bugs</td>
<td>19%</td>
</tr>
<tr>
<td>RTL better than hand-coded</td>
<td>14%</td>
</tr>
<tr>
<td>Faster ECO implementation</td>
<td>8%</td>
</tr>
<tr>
<td>Better product differentiation</td>
<td>7%</td>
</tr>
<tr>
<td>Other</td>
<td>4%</td>
</tr>
</tbody>
</table>

Productivity

QoR
## Typical Industry HLS experience

**Presented at SystemC conference Japan 2010**

<table>
<thead>
<tr>
<th>Design</th>
<th>Hand written RTL [cell area]</th>
<th>1st trial HLS</th>
<th>Final HLS results</th>
<th>Number of lines</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[cell area]</td>
<td>Compare to hand design</td>
<td>[cell area]</td>
<td>Compare to hand design</td>
</tr>
<tr>
<td>DesignA</td>
<td>92,187</td>
<td>139,581</td>
<td>1.51</td>
<td>97,479</td>
</tr>
<tr>
<td>DesignB</td>
<td>94,248</td>
<td>106,812</td>
<td>1.13</td>
<td>71,982</td>
</tr>
<tr>
<td>DesignC</td>
<td>1,053,981</td>
<td>5,381,658</td>
<td>5.11</td>
<td>923,508</td>
</tr>
<tr>
<td>DesignD</td>
<td>131,193</td>
<td>163,026</td>
<td>1.24</td>
<td>124,407</td>
</tr>
<tr>
<td>DesignE</td>
<td>280,809</td>
<td>533,115</td>
<td>1.90</td>
<td>268,812</td>
</tr>
<tr>
<td>DesignF</td>
<td>402,624</td>
<td>636,145</td>
<td>1.58</td>
<td>419,733</td>
</tr>
</tbody>
</table>

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- **HLS Synthesis has the same learning curve as RTL development.**

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HLS benefits

• Simulation 10-1000x faster
• Hardware/Software co-dev
• High Level Model (HLM) re-use
• End Results:
  • Less engineering time
  • Max IP value, better re-use
  • Faster TTM
• Increased productivity
  • With higher abstraction
• QoF close to/better than RTL
• Faster debug and verification
Keys to Raising Abstraction

- Implicit state machine
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  - Leaves room for exploration
- Design exploration
  - Same source can produce designs for different purposes
- Array handling
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Thank you for your time!